



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/944,732

08/31/2001

Lee John Smith

GOO79

2003

23513

7590

01/11/2005

GUNNISON MCKAY & HODGSON, LLP
GARDEN WEST OFFICE PLAZA, SUITE 220
1900 GARDEN ROAD
MONTEREY, CA 93940

EXAMINER

GRAYBILL, DAVID E

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/944,732

Applicant(s)

SMITH ET AL.

Examiner

David E Graybill

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 26-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 26-34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 26-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Shin (2004/0007771).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In the abstract, and at paragraphs 24, 30, 35-37, 64-71, 110-114, and claims 8-10, Shin discloses the following:

A semiconductor package comprising: a substrate 10 having opposing first and second surfaces and a rectangular (the rectangular cross section of the opening illustrated in Fig. 2A) through hole 14 extending through the

Art Unit: 2822

substrate between the first and second surfaces, said rectangular through hole having four sides (right, left, top and bottom); a first conductive circuit pattern 19 disposed on the first surface of the substrate, and a second conductive pattern 19 disposed on the second surface of the substrate, wherein the first conductive circuit pattern includes at least "bond fingers" (illustrated but not labeled) and lands 13, the second conductive pattern includes at least lands 13, and at least some of the first and second circuit patterns are electrically coupled 14 through the substrate; a first semiconductor chip 2 having opposed active and inactive surfaces, wherein the first semiconductor chip is disposed within the through hole without contacting the substrate, and the active surface of the first semiconductor chip includes bond pads 2a; a second semiconductor chip 1 having opposed active and inactive surfaces, wherein the second semiconductor chip is disposed within or over the through hole without contacting the substrate, and the active surface of the second semiconductor chip includes bond pads 1a, wherein the inactive surface of the second semiconductor chip faces and is mounted on the active surface of the first semiconductor chip so that the active surfaces of the first and second semiconductor chips are oriented in a same direction; a plurality of first conductive wires 20, wherein each of the first conductive wires electrically connects a respective one of the bond pads of the first semiconductor chip to a respective one of the bond fingers of the

first conductive circuit pattern; a plurality of second conductive wires 20, wherein each of the second conductive wires electrically connects a respective one of the bond pads of the second semiconductor chip to a respective one of the bond fingers of the first conductive circuit pattern circuit pattern, at least some of said first and second conductive wires being electrically connected to bond fingers located adjacent a first side (the left side) of the rectangular through hole, and at least some of said first and second conductive wires being electrically connected to bond fingers located adjacent a second side (the right side) of the rectangular through hole, the first and second sides of the through hole being opposite one another; and an encapsulant 30 filling the through hole and contacting the first surface of the substrate, the bond fingers of the first conductive circuit pattern, the first semiconductor chip, the second semiconductor chip, and the first and second conductive wires, wherein the inactive surface of the first semiconductor chip is exposed through the encapsulant in a common plane with the second surface of the substrate ("the second surface of the substrate and the inactive surface of the second semiconductor chip being in a common horizontal plane"), and the lands of the first and second conductive circuit patterns are uncovered by the encapsulant; wherein the inactive surface of the second semiconductor chip has a smaller area than the active surface of the first semiconductor chip; wherein the first and

second semiconductor chips are a same size; a plurality of conductive balls 40, wherein each of the conductive balls is fused to a respective one of the lands of the second conductive circuit pattern, and the active surfaces of the first and second semiconductor dies are oriented in a same direction as the first surface of the substrate; wherein each of the conductive balls is fused to a respective one of the lands of the first conductive circuit pattern, and the active surfaces of the first and second semiconductor dies are oriented in a same direction as the first surface of the substrate.

Claims 26-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (2004/0007771).

Shin is applied as it is applied supra.

Although Shin does not appear to literally disclose a rectangular through hole, said rectangular through hole having four sides, as cited, Shin explicitly discloses that the chips are rectangular. Moreover, in view of this disclosure of Shin, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose a rectangular through hole because it could compactly conform the through hole to the chip shape. In any case, applicant has not disclosed that, in view of the applied prior art, the shape is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the product

would possess utility using another shape. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

For information on the status of this application applicant should check PAIR:

Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you

Art Unit: 2822

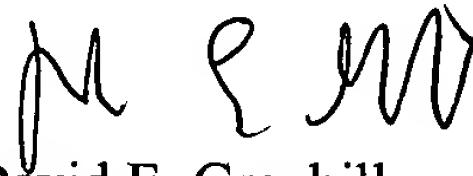
have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours:

Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.



David E. Graybill
Primary Examiner
Art Unit 2827

D.G.

9-Jan-05